IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

Deep-level transient spectroscopic studies of ZnSe - GaAs heterointerfaces

This article has been downloaded from IOPscience. Please scroll down to see the full text article.

1997 J. Phys.: Condens. Matter 9 995

(http://iopscience.iop.org/0953-8984/9/5/006)

View the table of contents for this issue, or go to the journal homepage for more

Download details:
IP Address: 171.66.16.207
The article was downloaded on 14/05/2010 at 06:14

Please note that terms and conditions apply.

J. Phys.: Condens. Matter **9** (1997) 995–1004. Printed in the UK PII: S0953-8984(97)75499-7

Deep-level transient spectroscopic studies of ZnSe–GaAs heterointerfaces

F Lu, S K Zhang, J Wang, Z S Li, L Ke, J B Wang, H H Sun and X Wang
Surface Physics Laboratory and Fudan T D Lee Physics Laboratory, Fudan University, Shanghai 200443, People's Republic of China

Received 18 June 1996, in final form 6 November 1996

Abstract. A numerical analysis of the deep-level transient spectroscopy of the ZnSe–GaAs heterojunction based on rigorously solving the Poisson equation and taking account of the interfacial band discontinuity is presented. By combining the numerical analysis with the experimental measurements, properties of the interfacial defects are revealed. It is found that there are donor-like interfacial defects at the ZnSe–GaAs interface with the energy level being located at about 0.5 eV below the conduction band minimum of GaAs, and with an electron capture cross section of 2.5×10^{-16} cm^2. The areal density of interfacial defects is determined to be 1×10^{12} cm^2 for ZnSe grown on GaAs substrate treated with S_2Cl_2.

1. Introduction

Since the successful achievement of a blue–green laser in recent years, the ZnSe-based II–VI compound semiconductors have attracted a great deal of attention in semiconductor physics and device research. In growing ZnSe-based quantum well structures, the substrates used are mostly (100) GaAs wafers. Although the lattice mismatch between ZnSe and GaAs is small (0.27%), the introduction of misfit dislocations near the heterointerface will occur when the thickness of the epitaxial layer increases beyond a critical thickness. In addition, there exists a valence mismatch at the heterointerface between ZnSe and GaAs, which will inevitably cause the creation of interfacial defects. It is well established that the poor operation lifetime of the II–VI semiconductor blue laser to date is basically due to the degradation of crystalline quality of epilayers caused by the dislocation penetration in the quantum well laser structure. It is thus important to investigate the interfacial defects of the ZnSe/GaAs system. In addition to the direct observation of dislocations by the electron microscope, electrical measurements are important for providing substantial information concerning the defect properties. Several groups have attempted to study the interface characteristics of ZnSe–GaAs heterostructures by capacitance–voltage (C–V) measurements [1–3]. The basic results obtained from the high-frequency C–V characteristics are not informative enough, since the metal–ZnSe–GaAs was treated as a MIS structure, which is approximately correct if the heterojunction is a p-ZnSe–p-GaAs structure since the large valence band offset enables the wide-gap ZnSe layer to be considered as an insulator. In the case of n-ZnSe–n-GaAs, the conduction band offset is too small to be considered as a potential barrier, so the MIS model is not valid. Moreover, the MIS C–V measurements usually only give a U-shaped distribution of interface states using Terman's method [4], which is a classical and also crude technique even for the SiO_2–Si system. The defect levels induced by the lattice mismatch

 © 1997 IOP Publishing Ltd

and chemical mismatch have not been identified by the C–V measurements. Matsumoto *et al* [5] first used deep-level transient spectroscopy (DLTS) to observe the electron traps in the n-ZnSe–n-GaAs heterojunction. The ZnSe epitaxial layers which they grew were partially strain relaxed, so several electron traps with different activation energies were observed and most of them originated from the bulk rather than from the interfaces. The assignment of the interfacial defects in their work does not seem to be unambiguous since the bias voltage corresponding to the position of the interface was defined by the C–V electron concentration profile without taking into account the conduction band offset at the heterointerface. Hariu *et al* [6] proposed a new DLTS analysis method, by which the defect-related surface states were revealed when the density of surface states with a U-shaped distribution was reduced down to 10^{11} cm^{-2} eV^{-1}. However, the MIS model was still used as the basis of the data analysis. In this work, we present a detailed numerical analysis of the DLTS data based on solving rigorously the Poisson equation and taking into account the interfacial band offset. The unambiguous identification of the interfacial defect states and determinations of their energy levels, densities and cross sections are achieved.

2. Principle of measurements

2.1. Variation of electron density on interfacial defects with applied voltage

In an Al–n-ZnSe–n-GaAs sample structure, if there existed interfacial defects, the electron population on the defect level would be determined by the relative positions of the defect level E_t and the quasi Fermi level E_{fn}. The calculation of $E_t - E_{fn}$ at the interface could be performed by solving numerically the Poisson equation and taking into account the band discontinuity at the ZnSe–GaAs interface. The continuous boundary condition at the interface is influenced by the interfacial charge density. In the case of donor-like defects, the boundary condition is

$$\varepsilon_0\varepsilon_2 E_2 = \varepsilon_0\varepsilon_1 E_1 + q(N_s - n_t) \quad (1)$$

where ε_1 and ε_2 are the relative dielectric constants of the materials at the two sides of the interface, E_1 and E_2 are the electric fields at the two sides, ε_0 is the permittivity of vacuum, q is the electron charge, N_S is the areal density of interfacial defects, and n_t is the areal electron density in the defect level. If the defects are acceptor-like, the boundary condition becomes

$$\varepsilon_0\varepsilon_2 E_2 = \varepsilon_0\varepsilon_1 E_1 - qn_t. \quad (2)$$

The calculated conduction bands of the heterojunction with respect to the quasi-Fermi level E_{fn} under different bias voltages are shown in figure 1. The parameters used in the calculations are as follows. The doping concentrations in n-ZnSe and n-GaAs are 1×10^{15} and 1×10^{16} cm^{-3}, and the dielectric constants of ZnSe and GaAs are 9.25 and 11.5, respectively. The thickness of the ZnSe layer is 100 nm. The conduction band offset is taken to be $\Delta E_c = -0.1$ eV, where the negative value means that the conduction band edge of ZnSe is located below that of GaAs at the heterointerface. The energy level is set as 0.5 eV below the conduction band minimum of the GaAs and the density of donor-like interfacial defects is $N_s = 1 \times 10^{12}$ cm^{-2}. The Schottky barrier height between Al and ZnSe is chosen as 0.76 eV [7]. The band diagram of the structure under $V_R = 0$ is shown in the inset of figure 1.

It can be seen from figure 1 that the defect level E_t is located below the Fermi level E_{fn} under zero bias or forward bias, and as the reverse bias increases E_{fn} moves downwards

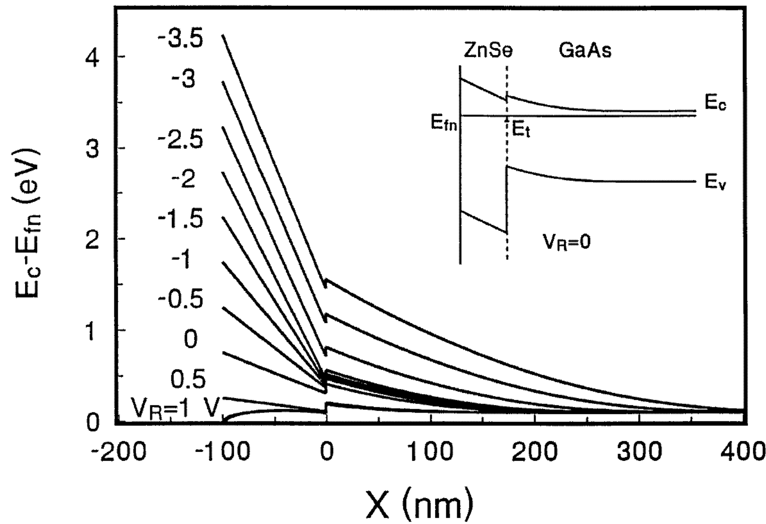


Figure 1. The calculated conduction band of the heterojunction under different bias voltages.

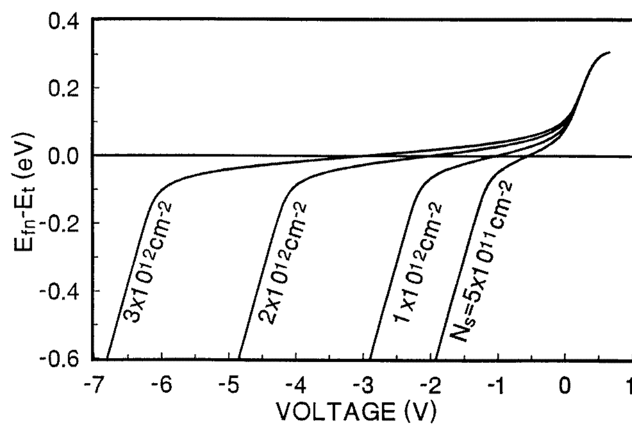


Figure 2. The variation of $E_{fn} - E_t$ with bias voltage for different defect densities.

with respect to E_t and the electron population on the defect level changes. If the density of defect were large, the Fermi level would be pinned at E_t as the reverse bias increased until the electrons on the defect level were fully depleted. Figure 2 shows the variation of $E_{fn} - E_t$ with bias voltage for different defect densities. Figure 3 gives the variation of electron densities on the defect level with the applied voltage for different defect densities.

If the interfacial defects are of acceptor type, a similar argument can be derived, but the electrons on the defect level will be depleted under lower reverse bias voltage, provided the energy level and the density of interfacial defects are the same as that of donor-like defects. Figure 4 shows the comparison of the energy bands under zero bias voltage for the cases of donor-type defects (a) and acceptor-type defects (b). The variations of electron densities on the acceptor-type defect level are also shown as the inset in figure 3.

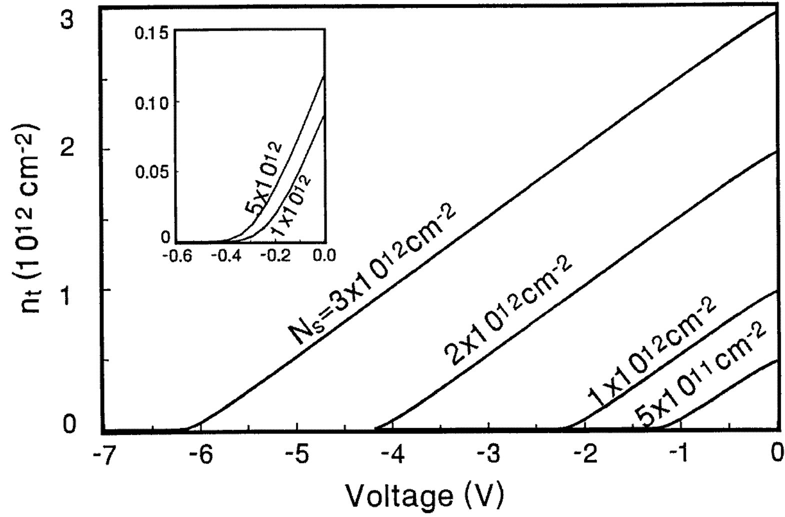


Figure 3. The variation of electron densities on the defect level with the applied voltage for different defect densities. The case for acceptor-like defects is given in the inset.

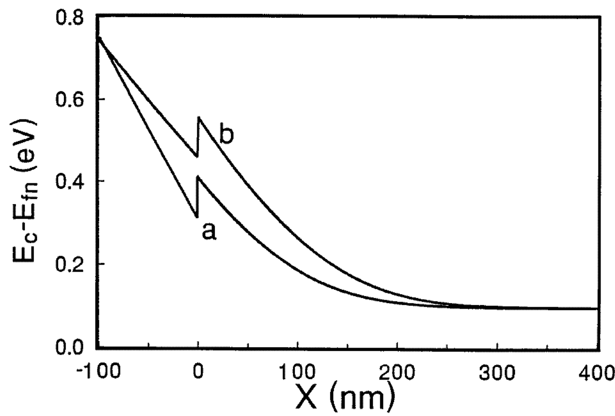


Figure 4. The comparison of the energy bands under zero bias voltage for the cases of donor-type defects (a) and acceptor-type defects (b).

It can be seen from figure 3 that it is easier to deplete the electrons on the acceptor-type defects than that on the donor-type defects, therefore these two kinds of defect could be distinguished according to the bias voltage necessary to fully deplete the electrons on the defect level.

2.2. *The transient variation of electron density on the defect level*

Suppose that E_t were located above the midgap of the forbidden band; in an n-type semiconductor the time dependence of electron density on the defect level after a sudden

change of applied voltage could be derived by the Shockley–Read–Hall theory [8]:

$$\frac{\partial n_t}{\partial t} = C_n(N_S - n_t) - e_n n_t \tag{3}$$

where C_n and e_n are the capturing rate and the emission rate of electrons, respectively.

When the reverse applied voltage jumps from low to high at $t = 0$, the electron density on the defect level is tentatively larger than its steady value at high voltage. Thus the carrier emission from E_t dominates the process. The solution of (3) is

$$n_t(t) = n_t(0)\exp(-e_n t) \tag{4}$$

where $n_t(0)$ is the initial electron density on the defect level.

On the other hand, when the reverse bias jumps from high to low at $t = 0$, the first term is much larger than the second term in (3). The variation of electron density follows the relation

$$N_S - n_t(t) = [N_S - n_t(0)]\exp(-C_n t). \tag{5}$$

2.3. The DLTS signal originated by the electron emission from the interfacial defect level

For an Al–n-ZnSe–n-GaAs structure with relatively thin ZnSe layer and lower doping concentration, the carriers in ZnSe are already depleted under zero bias and the space charge region of the Schottky barrier is extended into the GaAs substrate. The total capacitance C of this structure is the series of a capacitance of ZnSe layer C_1, and a capacitance of the GaAs space charge region C_2.

$$1/C = 1/C_1 + 1/C_2 = d/A\varepsilon_1\varepsilon_0 + W/A\varepsilon_2\varepsilon_0 \tag{6}$$

where A is the sample area, d is the thickness of ZnSe, W is the width of the GaAs space charge region, and ε_1 and ε_2 are the relative dielectric constants of ZnSe and GaAs, respectively

A jump of the reverse bias from low to high will cause the emission of electrons from the defect level. Suppose the charge variation by the electron emission at the interface of ZnSe–GaAs is ΔQ_s; correspondingly, the variations of voltages across the ZnSe layer and the GaAs space charge region are

$$\Delta V_1 = (\Delta Q_s)/C_1 \tag{7}$$

and

$$\Delta V_2 = (1/C_1 + 1/C_2))qN_D\,\Delta W \tag{8}$$

respectively. Since the total applied voltage does not change after $t = 0$,

$$\Delta V_1 + \Delta V_2 = 0. \tag{9}$$

By combining (7)–(9), we obtain

$$\Delta W = -(C/qN_D C_1)\,\Delta Q_S. \tag{10}$$

From (6), the variation of the sample capacitance is

$$\Delta C = -(C^2/A\varepsilon_0\varepsilon_2)\,\Delta W = (C^3/qN_D C_1 A\varepsilon_0\varepsilon_2)\,\Delta Q_S. \tag{11}$$

According to (4), ΔQ_S could be written as

$$\Delta Q_S(t) = q\,\Delta n_t \exp(-e_n t) \tag{12}$$

and therefore

$$\Delta C(t) = (C^3\Delta n_t/A\varepsilon_0\varepsilon_2 C_1 N_D)\exp(-e_n t). \tag{13}$$

During the DLTS measurement, the difference between the values of $\Delta C(t)$ at two fixed times t_1 and t_2 on each $\Delta C(t)$ curve gives the DLTS signal S, i.e.

$$S = \Delta C(t_1) - \Delta C(t_2) = (C^3 \Delta n_t / A\varepsilon_0\varepsilon_2 C_1 N_D)[\exp(-e_n t_1) - \exp(-e_n t_2)]. \tag{14}$$

When the temperature scans, passing a point where $e_n = \ln(t_2/t_1)/(t_2 - t_1)$, then S reached a maximum S_m. If we choose $t_2 = 2t_1$, then

$$S_m = C^3 \Delta n_t / 4A\varepsilon_0\varepsilon_2 C_1 N_D. \tag{15}$$

If we set the pulse voltage to let the defect level be filled with electrons during the 'on' period (low reverse bias) and let the electrons on the defect level be fully emitted during the 'off' period (high reverse bias), $\Delta n_t = N_S$, and the defect density can be derived from (15) as

$$N_S = (4A\varepsilon_0\varepsilon_1\varepsilon_0\varepsilon_2 N_D / C^3 d) S_m. \tag{16}$$

The height of the DLTS peak depends also on the width of the applied pulse voltage. By fixing the value of the rate window and carrying out the temperature scans at different pule widths, one can obtain a set of DLTS peaks. The capturing rate C_n can be derived from the slope of the $\ln[1 - S_m(t)/S_m(\infty)]$–$t_p$ relation. The electron cross section of the defect level σ_n is related to C_n by the following expression:

$$C_n = \sigma_n v_t n_s \tag{17}$$

where n_s is the electron concentration in the conduction band at the interface and v_t is the thermal velocity of electrons.

3. Experimental details

The sample was grown by molecular beam epitaxy (MBE) on a GaAs(100) wafer. The substrate was an n–n^+ structure with the n-type GaAs epitaxial layer grown on an n-substrate using liquid phase epitaxy. The doping concentration in the n-layer was 1×10^{16} cm^{-3}. The GaAs wafer was treated sequentially by ultrasonic cleaning in acetone, ethanol, and deionized water for 5 min each. In order to improve the interface quality between the ZnSe epitaxial layer and the GaAs substrate, the GaAs surface was treated with sulphur passivation before the growth of the ZnSe film. The passivation method used in this experiment is S_2Cl_2 treatment [9]. The wafer was dipped in a solution of S_2Cl_2:CCl_4 = 1:4 for 20 s and then rinsed by CCl_4, acetone, ethanol, and deionized water, followed by blowing dry in N_2. After being loaded into the MBE growth chamber, the wafer was heated in the vacuum to 380 °C for 10 min in order to remove the extra sulphur, leaving the GaAs surface terminated by S–Ga or S–As bonds. The formation of a Ga-enriched GaAs surface, which usually occurs in the conventional surface treatment, could thus be avoided.

The MBE growth of ZnSe was carried out at the temperature of 280 °C using two effusion cells containing pure elemental Se (6N) and Zn (6N) sources. The partial pressure of Se is larger than that of Zn by a factor of two to maintain the stoichiometry in the epilayer. The growth rate was about 0.1 nm s^{-1}. The thickness of the ZnSe epilayer is about 100 nm, which is smaller than the predicted critical thickness of pseudomorphic growth.

The ohmic contact to the sample was prepared by evaporating In on its back side and a Schottky contact on its front side was formed by evaporating an Al dot with a diameter of 1 mm. The DLTS measurements were carried out in the temperature range of 77–370 K.

4. Results and discussion

4.1. The defect and its spatial location

In figure 5, (a)–(d) show the DLTS spectra of the sample under different reverse bias voltages V_R and a fixed height of filling pulse $V_P - V_R = 1$ V. Only a single DLTS peak is observed in the temperature range of 77–370 K. For comparison, the DLTS measurement was also performed for an Al–GaAs sample made from the same n–n$^+$ GaAs wafer. No DLTS signal could be seen. This illustrates that the defect signal does not originate from the GaAs substrate. To further exclude the possibility that the defect signal originates from the GaAs substrate during MBE growth, a positive bias of 1 V was applied for DLTS measurement. Under this condition, the GaAs substrate is not included in the space charge region of the Schottky barrier as seen from figure 1. It is thus expected that the DLTS peak in figure 5 should disappear or be greatly suppressed if it originates from the GaAs region. However, the experiment still gives a similar peak as shown by curve (e) in figure 5. The shift of this defect peak towards lower temperature will be explained later. On the other hand, since the ZnSe layer is unintentionally doped and its thickness is only about 100 nm, it is fully depleted and the space charge region of the Schottky contact extends into the GaAs substrate even at zero and reverse bias voltages. Therefore, the DLTS signal, instead of originating from the ZnSe epilayer, really has its origin in the interface of ZnSe–GaAs.

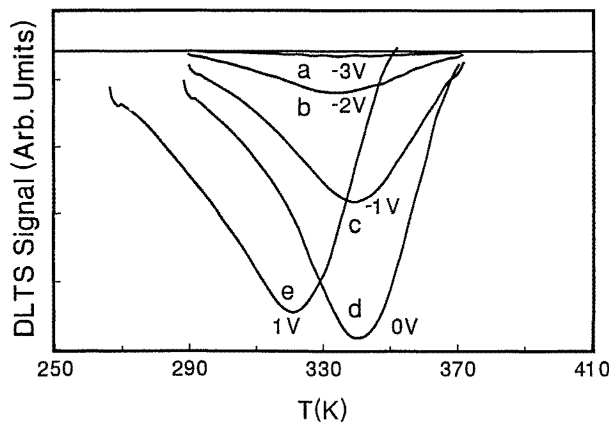
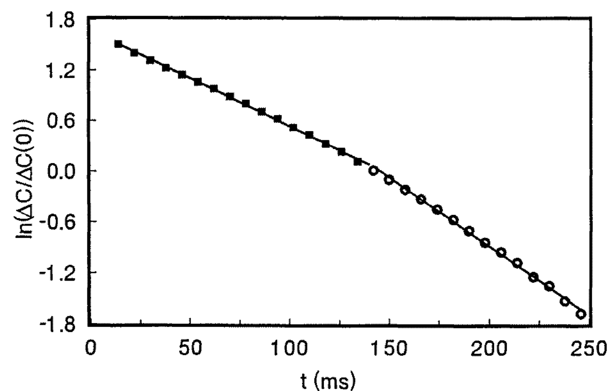
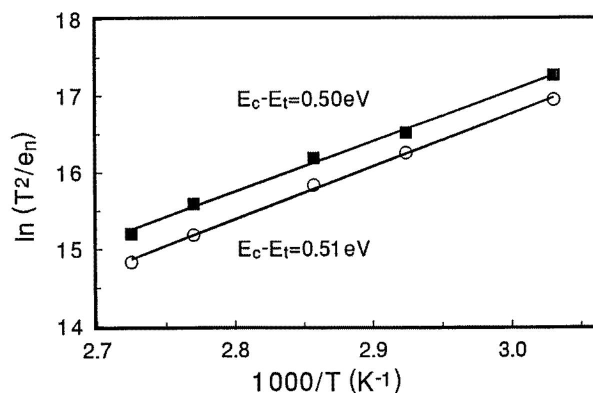


Figure 5. The DLTS spectra under different reverse bias voltage V_R: (a) −3 V; (b) −2 V; (c) −1 V; (d) 0 V; (e) 1 V. The pulse voltage was fixed at $V_P - V_R = 1$ V.

In the case of bulk materials, the DLTS peak height versus bias voltage gives information on the spatial distribution of traps across the regions swept over by the edge of the space charge region during the variation of bias. In figure 5, the peak height increases dramatically when the bias voltage changes from −3 to 0 V. This means there must be a monotonic increase of trap concentration from the GaAs bulk towards the interface, if the DLTS peak is attributed to the bulk traps in GaAs and the effect of the heterointerface is ignored. However, it is difficult to explain the formation of such a non-uniform defect profile. A reasonable explanation of figure 5 based on our interfacial defect model is given as follows. According to the calculated results shown in figure 3, if the interfacial defects were located at $E_c - E_t = 0.5$ eV with the density $N_S = 1 \times 10^{12}$ cm^{-2} (the values of E_t and N_s will be confirmed experimentally below), the Fermi level E_{fn} at the interface would be located



(a)



(b)

Figure 6. The $\ln(\Delta C/\Delta C(0))$–$t$ plot (a) and the corresponding $\ln(T^2/e_n)$–T plot (b) obtained from the transient capacitance spectrum.

below $E_c - 0.5$ eV when the applied reverse bias voltage was larger than 2 V, so the electron density n_t was almost zero. Therefore no DLTS signal is observed in figure 5(a). When the reverse bias voltage changes from -2 to 0 V, n_t increases monotonically, and the DLTS peak height increases accordingly. From the agreement between the theoretical prediction and the experimental observation, it is reasonable to attribute the DLTS peak in figure 5 to donor-type interfacial defects.

4.2. Defect energy level

The activation energies of peaks (b), (c) and (d) in figure 5 could be determined by measuring the DLTS spectra under different rate windows. The results are 0.51, 0.50 and 0.49 eV, respectively. This means that the DLTS peak does not shift significantly in the measured temperature range under different reverse bias voltages, and the defect states are distributed in a very narrow energy range or even could be regarded as a single level. This is quite different with the previous results, where a U-shaped distribution of interfacial states in energy was found at the MIS-type ZnSe–GaAs heterointerface [1].

The defect energy level could also be determined by measuring the capacitance transient

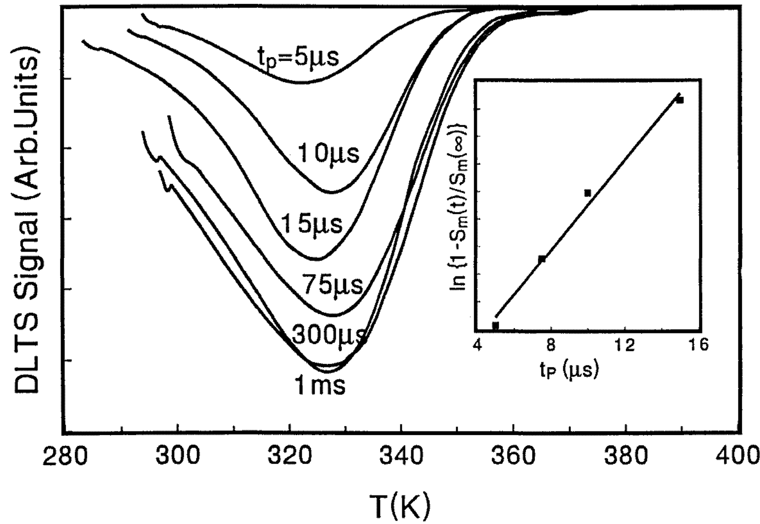


Figure 7. The DLTS spectra for different pulse widths. The inset shows the Arrhenius plot $\ln[1 - S_m(t)/S_m(\infty)] - t_p$.

of the sample at different temperatures under zero bias after applying a pulse voltage with the height of 1 V and the width of 1 ms. Figure 6(a) is a $\ln(\Delta C/\Delta C(0))$–$t$ plot measured at 340 K, where $\Delta C(0)$ is the capacitance change at $t = 0$. It consists of two linear sections, from which the emission rates e_n can be determined. The $\ln(T^2/e_n)$–T plot is shown in figure 6(b). The slopes give the activation energies of 0.50 and 0.51 eV, which coincide fairly well with the above DLTS results.

4.3. Defect density

Experiments indicate that the DLTS signal reaches a maximum at $V_R = -3$ V and $V_p - V_R = 4$ V. From figure 3 it can be seen that the defect level is empty under the reverse bias of -3 V and is almost fully occupied under zero or positive bias. So the conditions above could fulfil the requirement of measuring N_S described in subsection 2.3. By taking the measured S_m and substituting it and other parameters of the sample into (16), the density of interfacial defects is determined to be $N_S = 9.8 \times 10^{11}$ cm^{-2}.

4.4. The cross section

By measuring the DLTS spectra under different pulse widths, as shown in figure 7, the capture rate C_n of the defect level is obtained from the slope of the Arrhenius plot $\ln[1-S_m(t)/S_m(\infty)]$–$t_p$, as shown in the inset of figure 7. In order to obtain the cross section σ_n, one needs to know the electron concentration n_S at the interface, which is determined by the position of quasi-Fermi-level E_{fn} during the pulse period. The calculation of n_S here differs from that for the case of bulk deep levels. In the latter case, n_S is simply determined by the doping concentration. However, in the case of heterointerfacial defects, n_S must be obtained by solving numerically the Poisson equation with the parameters derived experimentally. In our case, E_{fn} is found to be at 0.31 eV below the conduction band minimum of ZnSe under the pulse voltage. From the DLTS peak temperature in figure 7,

n_S is estimated to be 2.3×10^{13} cm^{-3}. The capture rate derived above is $C_n = 1.6 \times 10^5$ s^{-1}, thus the electron capture cross section calculated from (17) is $\sigma_n = 2.5 \times 10^{-16}$ cm^2. To our knowledge, this is the first time that the value of σ_n has ever been given for the interfacial defects in a ZnSe–GaAs heterojunction.

4.5. The effect of S_2CL_2 passivation

It was found by Wu *et al* [10] that the S passivation of the GaAs substrate can improve the interface quality in the heteroepitaxial growth of ZnSe. The S_2Cl_2 passivation technique was found to be superior to the ordinary $(NH_4)_2S_x$ treatment [9]. To make a comparison, another ZnSe–GaAs sample was prepared with the same structure and growth conditions as the previous one, except the GaAs substrate was dipped in $(NH_4)_2S_x$ aqueous solution at 60 °C for 30 min. Its DLTS peak height is about twice that of the S_2Cl_2 treated sample. The parameters of the defect are determined to be $E_t = E_c - 0.59$ eV to $E_t = E_c - 0.49$ eV, $N_S = 2 \times 10^{12}$ cm^{-2}, and the defect is also donor-like.

5. Conclusions

By analysing numerically the DLTS data, we are able to study quantitatively the properties of the interfacial defects at the n-ZnSe–n-GaAs heterojunction grown pseudomorphically by MBE. The energy level, areal density, and capture cross section of the defects are determined experimentally. It is found that S_2Cl_2 treatment of the GaAs substrate before epitaxial growth can reduce the defect density by a factor of two as compared with that of an ZnSe–GaAs interface grown on a GaAs substrate treated with $(NH_4)_2S_x$.

Acknowledgment

This work was supported by the Key Project of the State Commission of Science and Technology.

References

[1] Qian Q D, Qiu J, Melloch M R, Cooper J A, Kolodziejski J L A, Kobayashi M and Gunshor R L 1989 *Appl. Phys Lett.* **54** 1359
[2] Murawala P A, Tsuji Q and Fujita S 1991 *Japan. J. Appl. Phys.* B **30** 3777
[3] Matsumoto T, Kobubo N, Kawakami K and Kato T 1992 *J. Crystal Growth* **117** 578
[4] Terman M L 1962 *Solid State Electron* **5** 285
[5] Matsumoto T, Ito Y and Ishida T 1989 *Japan. J. Appl. Phys.* **28** 541
[6] Hariu T, Yamauchi S, Tanaka H and Ono S 1991 *Appl. Surf. Sci.* **48/49** 204
[7] Sze S M 1981 *Physics of Semiconductors Devices* (New York: Wiley) p 204
[8] Shockley W and Read W T 1952 *Phys. Rev.* **87** 835
[9] Li Z S, Cai W Z, Su R Z, Dong G S, Huang D M, Ding X M, Hou X Y and Wang X 1994 *Appl. Phys. Lett.* **64** 3425
[10] Wu Y H, Toyoda T, Kawakami Y and Fujita S 1990 *Japan. J. Appl. Phys.* **29** 144